WHAT IS CLAIMED IS:

1. A timing analysis apparatus for performing timing analysis of a semiconductor integrated circuit based on inputted circuit information, comprising:

a coefficient arithmetically operating unit for calculating variation coefficients of delay time in a target path being an analysis target with a variation in delay time in each gate being cancelled out in accordance with a number of gate stages in the target path in the semiconductor integrated circuit; and

a first timing analysis unit for performing timing analysis in the target path based on the calculated variation coefficients and the circuit information.

2. The timing analysis apparatus according to claim 1,

wherein said coefficient arithmetically operating unit comprises a coefficient of the number of stages arithmetically operating section for calculating coefficients of the number of stages indicating variation amounts in delay time according to the number of gate stages in the target path based on the circuit information,

a variation width arithmetically operating section for calculating a variation width of delay time in the entire target path based on the circuit information, and

a variation coefficient arithmetically operating section for calculating the variation coefficients of the delay time in the target path based on the calculated coefficients of the number of stages and the variation width of the delay time.

3. The timing analysis apparatus according to claim 2, further comprising:

a table of coefficients of the number of stages in which an optional number of gate stages in a path and the coefficients of the number of stages are made to correspond to each other,

wherein said coefficient of the number of stages arithmetically operating unit obtains the coefficients of the number of stages according to the number of gate stages in the target path with reference to said table of the coefficients of the number of stages.

4. The timing analysis apparatus according to claim 1, further comprising:

an information input unit for inputting the circuit information therein and extracting delay information relating to delay time of each gate in the target path from the circuit information,

wherein said coefficient arithmetically operating unit calculates the variation coefficients of the delay time in the target path based on the extracted delay information of each gate.

5. The timing analysis apparatus according to claim 1,

wherein said first timing analysis unit verifies whether previously specified timing conditions are satisfied in the target path or not, based on the calculated variation coefficients and the circuit information.

6. The timing analysis apparatus according to claim 5,

wherein the timing conditions are the conditions relating to setup time and hold time in the target path.

7. The timing analysis apparatus according to claim 1, further comprising,

a second timing analysis unit for performing timing analysis in the target path by accumulating a variation in the delay time of each gate in the target path, based on the circuit information; and

a determination unit for determining whether previously specified timing conditions are satisfied or not based on a result of timing analysis supplied from said second timing analysis unit,

wherein said coefficient arithmetically operating unit calculates the variation coefficients of the delay time in the target path only when it is determined that the timing conditions are not satisfied in said determination unit.

8. The timing analysis apparatus according to claim 7, further comprising:

an information input unit for inputting the circuit information therein and extracting delay information relating to the delay time of each gate in the target path,

wherein said second timing analysis unit performs timing analysis of the target path based on the extracted delay information of each gate.

9. A timing analysis method for performing timing analysis of a semiconductor integrated circuit based on inputted circuit information, comprising:

a delay information extracting step of having the circuit information inputted and extracting delay information relating to delay time of each gate in a target path being an analysis target in the semiconductor integrated circuit from the circuit information;

a coefficient arithmetically operating step of calculating variation coefficients of the delay time in the target path with a variation in the delay time in each gate being cancelled out in accordance with the number of gate stages in the target path based on the delay information extracted in said delay information extracting step; and

a first timing analysis step of performing timing analysis in the target path with use of the variation coefficients calculated in said coefficient

arithmetically operating step and the circuit information.

10. The timing analysis method according to claim 9, further comprising:

a second timing analysis step of performing timing analysis in the target path by accumulating the variation in the delay time of each gate in the target path based on the delay information extracted in said delay information extracting step; and

a determination step of determining whether previously specified timing conditions are satisfied or not based on an analysis result in said second timing analysis step,

wherein said coefficient arithmetically operating step is executed only when it is determined that the timing conditions are not satisfied in said determination step.

11. The timing analysis method according to claim 9,

wherein said coefficient arithmetically operating step comprises a coefficient of a number of stages arithmetically operating step of calculating coefficients of a number of stages showing variation amounts of delay time according to the number of gates in the target path based on the circuit information;

a variation width arithmetically operating step of calculating a variation width of delay time of the

entire target path based on the circuit information; and

a variation coefficient arithmetically operating step of calculating the variation coefficients of the delay time in the target path based on the coefficients of the number of stages calculated in said coefficient of the number of stages arithmetically operating step and the variation width of the delay time calculated in said variation width arithmetically operating step.

12. A program product for making a computer execute:

a delay information extracting step of extracting delay information relating to delay time of each gate in a target path being an analysis target in a semiconductor integrated circuit from circuit information of the semiconductor integrated circuit;

a coefficient arithmetically operating step of calculating variation coefficients of delay time in the target path with a variation in the delay time in the each gate being cancelled out in accordance with a number of gate stages in the target path, based on the delay information extracted in said delay information extracting step; and

a first timing analysis step of performing timing analysis in the target path with use of the variation coefficients calculated in said coefficient

arithmetically operating step and the circuit information.

13. The program product according to claim 12 for making the computer execute:

a second timing analysis step of performing timing analysis in the target path by accumulating the variation in the delay time of each gate in the target path based on the delay information extracted in said delay information extracting step; and

a determination step of determining whether previously specified timing conditions are satisfied or not based on an analysis result in said second timing analysis step,

wherein only when it is determined that the timing conditions are not satisfied in said determination step, said program product makes the computer execute said coefficient arithmetically operating step.

14. The program product according to claim 12,

wherein said coefficient arithmetically operating step comprises a coefficient of a number of stages arithmetically operating step of calculating coefficients of a number of stages indicating variation amounts of delay time according to the number of gate stages in the target path based on the circuit information;

a variation width arithmetically operating step of calculating a variation width of delay time in the

entire target path based on the circuit information; and

a variation coefficient arithmetically operating step of calculating the variation coefficients of the delay time in the target path based on the coefficients of the number of stages calculated in said coefficient of the number of stages arithmetically operating step and the variation width of the delay time calculated in said variation width arithmetically operating step.

15. The program product according to claim 14,

wherein the coefficients of the number of stages according to the number of gate stages in the target path is obtained with reference to a table of the coefficient of the number of stages with an optional number of gate stages in a path and the coefficient of the number of stages being made correspond to each other, recorded in a recording medium.